ABSTRACT OF THE DISCLOSURE

A chip has a power bus, a first metal layer and a plurality of internal electronic circuits. The first metal layer has a plurality of power lines which are substantially parallel and electrically connected to the power bus in parallel for delivering electrical power to the internal electronic circuits. A plurality of metal lines of a second metal layer of the chip are configured by an automatic place and route (APR) process according to the internal electronic circuits, and at least one sparse area is formed on the second metal layer. Later, at least one supply-power area is configured in the sparse area, and is electrically connected to the power bus.